REMARKS

As a preliminary matter, it would be appreciated if the Examiner would make a hand annotation to the amendment submitted 16 December 2003 for this application to indicate the following correction. In the second full paragraph of the 16 December 2003 amendment, "electrically erasable read-only memory ("EPROM") region" should read "erasable programmable read-only memory ("EPROM") region".

The title has been shortened slightly.

The abstract has been revised to conform more closely to the pending claims.

Claims 23, 24, and 27 have been substantially rewritten in independent form. Claims 36 - 60, which variously depend from amended Claims 23, 24, and 27, have been added to claim the invention with more particularity. Claims 1 and 3 - 22 have been canceled without prejudice to pursue their subject matter in a continuation or divisional application. Accordingly, Claims 23 - 60 are now pending.

Claims 23 - 27 have been rejected under 35 USC 103(a) as obvious based on Hu, U.S. Patent 6,392,302 B1, and Lee, U.S. Patent Publication 2002/0001946 A1, taken with "applicants' admitted prior art", presumably the material disclosed in the Background section of the present application at pages 1 and 2, and Horiguchi et al. ("Horiguchi"), U.S. Patent Publication 2001/0002712 A1. This rejection is respectfully traversed.

Hu discloses a semiconductor fabrication technique in which cobalt layer 26 is deposited by physical vapor deposition, preferably sputtering, over upper polycrystalline silicon ("polysilicon") layer 18 of a gate stack suitable for use in an integrated circuit such as dynamic random-access memory ("DRAM"). Titanium layer 28 is deposited on cobalt layer 26. An anneal is performed to create cobalt silicide layer 30 from cobalt in cobalt layer 26 and silicon in upper polysilicon layer 18. The titanium and any unreacted cobalt are subsequently removed.

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Lee discloses a semiconductor fabrication technique in which titanium film 22 is deposited on semiconductor substrate 21 by ionized physical vapor deposition ("IPVD"), titanium nitride film 23 is formed on titanium film 22, and aluminum film 24 is formed on titanium nitride film 23. Aluminum film 24 functions as the primary interconnect metal for the metalization interconnect system.

The starting point for the Background material disclosed on pages 1 and 2 of the specification is a fixed-threshold insulated-gate field-effect transistor ("FET") having a doped polysilicon gate electrode and a pair of doped monocrystalline silicon ("monosilicon") source/drain regions. A cobalt layer is sputter deposited on top of the structure. A titanium layer is sputter deposited on the cobalt layer. An anneal is performed to create a cobalt silicide layer from cobalt in the cobalt layer and silicon in the gate electrode and the source/drain regions. The titanium layer and any unreacted cobalt are subsequently removed.

Horiguchi discloses a non-volatile semiconductor memory whose memory elements consist of floating-gate FETs, each having floating gate 5 and one or both of upper control gate 7 and side control gate 11. When control gates 7 and 11 are both present in each memory element, they can be connected together by electrically conductive cobalt silicide film 27. In that case, electrically conductive cobalt silicide films 25 and 26 are provided along the source/drain regions of the floating-gate FET in each memory element. With control gates 7 and 11 consisting of doped polysilicon and with the source/drain regions consisting of doped monosilicon, cobalt silicide layers 25 - 27 are created by depositing cobalt on the upper surface of the partially fabricated memory, performing a heat treatment to react part of the cobalt with underlying silicon, and removing unreacted cobalt.

Claims 23, 24, and 27, as rewritten in independent form, are repeated below:

23. A method comprising:

forming a cobalt layer over a body which comprises a silicon-containing erasable programmable read-only memory region;

forming a titanium layer over the cobalt layer by ionized physical vapor deposition;

reacting cobalt of the cobalt layer with silicon of a doped silicon section of the erasable programmable read-only memory region to form a cobalt silicide layer; and

substantially removing the titanium layer and any unreacted cobalt of the cobalt layer.

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24. A method comprising:

forming a cobalt layer over a body which comprises an erasable programmable read-only memory region that includes (i) a first section comprising doped monocrystalline silicon and (ii) a second section situated on the first section, an opening extending through the second section down to the first section;

forming a titanium layer over the cobalt layer by ionized physical vapor deposition;

reacting cobalt of the cobalt layer with silicon of the first section to form a cobalt silicide layer that contacts remaining material of the first section at the bottom of the opening; and

substantially removing the titanium layer and any unreacted cobalt of the cobalt layer.

27. A method comprising:

forming a cobalt layer over a body which comprises (a) a doped monocrystalline silicon substrate, (b) a floating gate overlying the substrate, (c) a control gate overlying the floating gate, and (d) electrically insulating material which surrounds the floating gate and separates the floating and control gates from each other and from the substrate;

forming a titanium layer over the cobalt layer by ionized physical vapor deposition;

reacting cobalt of the cobalt layer with silicon of the substrate to form a cobalt silicide layer that contacts remaining material of the substrate; and

substantially removing the titanium layer and any unreacted cobalt of the cobalt layer.

The Examiner appears to have a misconception as to what is disclosed in the Background section of the specification of the present application. With reference to Claims 23 - 27, the Examiner alleges on page 7 of the Office Action that the specification's Background material on pages 1 and 2 ("AAPA" as used by the Examiner) teaches in Figs. 1 and 2 and the related text "that the body comprises an erasable programmable read-only memory region (i.e. MOS)" and that "the cobalt silicide layer 210 is formed to contact a doped monocrystalline section 104 of programmable read-only memory region". This is incorrect.

The specification's Background section describes a fixed-threshold insulated-gate FET sometimes referred to as an "MOS" transistor or "MOSFET". However, an erasable programmable read-only memory ("EPROM") region is not the same as "MOS". While MOS transistors are employed in EPROMs, MOS transistors are also utilized in many other types of semiconductor devices.

Taking note of the fact that an EPROM is one type of non-volatile memory, nowhere does the specification's Background section refer to an EPROM or to any other type of non-volatile memory. Inasmuch as the MOS transistor described in the specification's

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Background section is of the fixed-threshold type, the specification's Background section does not disclose a variable-threshold FET suitable for use in a memory element of an EPROM. Contrary to what the Examiner alleges, the specification's Background section does not teach in Figs. 1 and 2 and the related text "that the body comprises an erasable programmable read-only memory region (i.e. MOS)". Nor does the specification's Background section teach that "the cobalt silicide layer 210 is formed to contact a doped monocrystalline section 104 of programmable read-only memory region".

The Examiner also seems to have a misconception as to what is disclosed in Horiguchi. With apparent reference to the disclosure in Hu that its semiconductor fabrication technique can be used in manufacturing DRAMs, the Examiner alleges on page 8 of the Office Action that a conventional "DRAM" would comprise a floating gate and a control gate as "evidenced" by Horiguchi. This is incorrect.

A floating-gate FET is utilized as a memory element in a non-volatile semiconductor memory, such as an EPROM, which retains the stored information when the memory's power is removed. A DRAM is a volatile semiconductor memory whose stored information is lost (evaporates) when the memory's power is removed. Although a random-access memory section is combined with an EPROM in some semiconductor memories, a DRAM itself does not normally utilize floating-gate FETs in its memory elements.

The background section of Horiguchi mentions DRAMs in one paragraph and, in a later paragraph, mentions flash memories that utilize floating-gate FETs. A flash memory is a type of EPROM. However, nowhere does Horiguchi state that a floating-gate FET is employed in a DRAM. Likewise, Horiguchi nowhere discloses any of its inventive semiconductor memories as being a DRAM.

Independent Claims 23 and 24 each recite that the body includes an EPROM region. As indicated above, EPROMs employ variable-threshold FETs, typically floating-gate devices. Since the Background section of the specification of the present application does not disclose a variable-threshold FET such as a floating-gate device, the specification's Background section does not disclose, or deal with, an EPROM region as specified in Claims 23 and 24.

Even if there were some motivation or suggestion for combining Hu and Lee with the specification's Background section, the combination would not teach the full subject matter

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of Claim 23 or 24. While Horiguchi does teach floating-gate FETs, Horiguchi does not disclose the use of titanium in forming cobalt silicide films 25 - 27. Hence, there would be no reason for applying Horiguchi to the attempted combination of Hu, Lee, and the specification's Background section. For this reason, Claims 23 and 24 are patentable over Hu, Lee, Horiguchi, and the specification's Background section. The same applies to Claims 25 and 26 since they respectively depend from Claims 24 and 23.

Independent Claim 27 recites particular details of a floating-gate FET. The comments made above about Horiguchi and the Background section of the specification of the present application in regard to Claims 23 and 24 carry directly over to Claim 27. For this reason, Claim 27 is allowable over Hu, Lee, Horiguchi, and the specification's Background section.

Claims 28 - 35 have been indicated as being allowable if rewritten in independent form. Claims 28 - 35 all depend (directly or indirectly) from Claim 27. Inasmuch as Claim 27 has been shown to be allowable over the applied art, Claims 28 - 35 are allowable in their present form.

New Claims 36 - 49 all depend (directly or indirectly) from Claim 27. New Claims 50 - 57 all depend (directly or indirectly) from Claim 23. New Claims 58 - 60 all depend (directly or indirectly) from Claim 24. Hence, dependent Claims 36 - 60 are patentable over Hu, Lee, Horiguchi, and the specification's Background section for the same reasons as Claims 23, 24, and 27.

In summary, Claims 23 - 27 and 36 - 60 have been shown to be patentable over the applied art. Claims 28 - 35 are allowable in their current form. Accordingly, Claims 23 - 60 should be allowed so that that application may proceed to issue.

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Respectfully submitted,

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